Amendments to the Specification:

Please replace the paragraph beginning at page 2, line 5, with the following amended paragraph:

Current flows vertically through MOSFET ~~MOSFT~~ 10 from the N+ drain 102 and through an N- drift region 106 and a channel region (denoted by the dashed lines) in P-body region 108 to the N+ source regions 110.

Please replace the paragraph beginning at page 5, line 24, with the following amended paragraph:

Figs. 14A-14C ~~Figs. 14A-14C~~ illustrate portions of stripe (open cell), square and hexagonal patterns in which the trenches and mesas can be formed in devices according to this invention.

Please replace the paragraph beginning at page 6, line 19, with the following amended paragraph:

A key innovation in **Fig. 2A** is the structure below the trench gate; the P-field ~~P- field~~ shield region 320 is laterally bounded by dielectric sidewalls 322 and bounded on the bottom by the PN junction with by N-region 318. This more general structure is illustrated in **Fig. 2B**. ~~As shown in Fig.2B,~~ P-field shield region 320 may be electrically biased either by shorting P-field shield region 320 to the top surface electrode of the N-region, as shown in **Fig. 2C**, or P-field shield region 320 may be biased independently with a separate voltage source, as shown in **Fig. 2B** . The contact with the top surface of the N-region can be either a Schottky barrier or an ohmic ~~contact~~ contact.

Please replace the paragraph beginning at page 6, line 27, with the following amended paragraph:

P-shield regions 320 can be formed by a selective epitaxial deposition after the RIE etch of the silicon and after the formation of a sidewall oxide. The basic structure shown in **Fig.** ~~**Fig**~~ **2B** is applied to a trench MOSFET (N+ substrate) and also IGBT (P+ substrate) structure in **Fig. 2A** ~~**Fig.2A**~~ to improve the blocking capability with thin gate oxide. The structure shown in **Fig. 2B** can be applied to make a low barrier height diode such as the

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Schottky barrier diode, as shown in **Fig. 2C** ~~Fig. 2C~~, or the vertical JFET structure, as shown in **Fig. 2D** ~~Fig. 2D~~. The devices shown in **Figs. 2A-2D** ~~Figs. 2A-2D~~ share the novel field shield structure, which is a P-region bounded by dielectric walls ~~dielectricwalls~~ on the sides and a PN junction below. The dielectric sidewalls prevent the spread of the P region ~~expansion~~ laterally by blocking the lateral diffusion of acceptors (e.g., boron) during device processing at high temperatures (e.g., above 800° C.). Of course, the polarities may be reversed in which case the field shield region would be formed of N-type material.

Please replace the paragraph beginning at page 7, line 8 (as previously amended), with the following amended paragraph:

Each of field shield regions 320 is connected to P-body regions 316 and N+ source regions 312 in the third dimension, outside the plane of the drawing. **Figs. 3A** and **3B** illustrate how this can be done. **Fig. 3A** is a cross-sectional view taken at the end of one of trenches 306 showing how field shield regions 320 can be connected to P-body regions 316 and N+ source regions 312. A P-well 328 is formed by ion implantation through a mask and diffusing a P-type dopant such as boron at the ends of trenches 306. As the P-type dopant diffuses, the P-well expands laterally under the sidewall spacers 322 and merges with the field shield regions 320. A P+ contact region 330 is formed beneath an opening in BPSG layer 324 at the surface of epi layer 304 to form an ohmic contact with metal layer 326. P+ contact region 330 can be formed during the same process step as P+ body contact region 314, shown in **Fig. 2A** ~~2~~. Since metal layer 326 is in electrical contact with N+ source regions 312 and P+ body contact regions 314 (see **Fig. 2A** ~~2~~), field shield regions 320 are likewise in electrical contact with N+ source regions 312 and P+ body contact regions 314.

Please replace the paragraph beginning at page 8, line 3, with the following amended paragraph:

Referring again to **Fig. 2A** ~~2~~, with this structure depletion regions form on both sides of dielectric sidewalls or sidewall spacers 322 when MOSFET 30 is turned off, with N+ substrate 302 biased positive with respect to source regions N+. This increases the

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avalanche breakdown voltage of the device and allows N drift region 318 to be doped more heavily, reducing the R_{ds}-on of MOSFET 30.

Please replace the paragraph beginning at page 8, line 8, with the following amended paragraph:

Figs. 4A-4H illustrate a process sequence that can be used to fabricate MOSFET 30. The process begins with the formation of epi layer 304 on top of N+ substrate 302. Because of the additional voltage blocking capability described above, epi layer 304 can be doped with an N-type dopant such as phosphorus to a concentration of 4×10^{16} cm^{-3} to 8×10^{16} cm^{-3}, for example, as compared with the normal doping concentration of 1×10^{16} cm^{-3} to 2.5×10^{16} cm^{-3} for a trench MOSFET with 30V breakdown . Prior to the process step illustrated in **Fig. 4A**, the structure is masked, and boron is implanted at a dose in the range of 1×10^{13} cm^{-2} ~~cm^{-3}~~ to 5×10^{13} cm^{-2} ~~cm^{-3}~~ to form P-wells, such as the P well 328 shown in **Fig. 3A, ~~3A~~** that are ~~is~~ used to contact the field shield regions.

Please replace the paragraph beginning at page 8, line 16, with the following amended paragraph:

A second photoresist mask is then formed over what is to be the active area of the device, and a thick field oxide layer (e.g., 0.2-1.0 μm thick) is thermally grown in what are to be the voltage termination regions (die edges) of the MOSFET. Then, as shown in **Fig. 4A**, a pad oxide layer 404 is thermally grown on the surface of epi layer 304 and a silicon nitride layer 402 is deposited over pad oxide layer 404. A third photoresist mask (trench mask) is formed atop nitride layer 402, and nitride layer 402 and oxide layer 404 are etched through openings ~~an opening~~ in the trench mask to form openings 406.

Please replace the paragraph beginning at page 9, line 1, with the following amended paragraph:

Referring to **Fig. 4D**, the exposed portions of sidewall spacers 322 are removed by isotropic oxide etch, typically diluted HF(hydrofluoric acid), leaving the field shield regions 320 and the portions of sidewall spacers 322 that are embedded between field shield regions 320 and N epi layer 304.

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Please replace the paragraph beginning at page 9, line 5, with the following amended paragraph:

As shown in **Fig. 4E**, gate oxide layer 310 is thermally grown on the exposed portions of the walls ~~and the floor~~ of trenches 408 and top surfaces of field shield regions 320, and the upper portion of trenches 408 are then filled with polysilicon gate 308, which is preferably heavily doped with an N-type dopant by ion implantation, POCl3 or *in situ*. The polysilicon typically covers ~~fills~~ the top surface of epi layer 304 and is etched back by using a fourth, polysilicon mask so that it is coplanar with the top surface of epi layer 304 (although typically the polysilicon is etched back slightly into the trenches).

Please replace the paragraph beginning at page 9, line 23, with the following amended paragraph:

As shown in **Fig. 4H**, metal layer 326 is deposited over the top surface of the structure to make an ohmic contact with N+ source regions 312 and P+ body contact regions 314. Metal layer 326 can be formed of Al:Si and can be from 1.3 to 5.0 μm thick. Typically a thin Ti/TiN barrier layer (not shown) is deposited under metal layer 326. The result is MOSFET 30, shown in **Fig. 2A** ~~2~~. A seventh photoresist mask (metal mask) is formed over metal layer 326, and metal layer 326 is etched through the metal mask to separate the portion of metal layer 326 ~~326S~~ that contacts N+ source regions 312 from the portion (not shown) that contacts the gate 308.

Please replace the paragraph beginning at page 10, line 1, with the following amended paragraph:

Figs. 5A-5G illustrate a process that can be used to form an alternative embodiment of the invention. This process can use as few as three masks and as many as seven masks. However, **Figs. 5A-5G** ~~Figs. 5A-5G~~ illustrate a three-mask version of the process . The process described above in **Figs. 4A-4C** is carried out, except that a blanket implant and diffusion to form P body region 316 is performed before pad oxide layer 404 and nitride layer 402 are deposited. As described above, trench mask is used to define the location of the trench. After field shield region 320 has been formed, as shown

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in **Fig. 4C**, pad oxide layer 404 and nitride layer 402 are left in place, as shown in **Fig. 5A**. The doping concentration of field shield region 320 may be in the range of 5 x 10^{16} to 5 x 10^{17} cm^{-3}, for example.

Please replace the paragraph beginning at page 10, line 11, with the following amended paragraph:

The exposed portions of oxide layers 322 are then removed. Gate oxide layer 310 is thermally grown on the exposed sidewalls of the trench and on the exposed upper surface of field shield region 320. The upper portion of trench 408 is then filled with polysilicon gate 308, which is preferably doped with an N-type dopant by ion implantation, POCl3, or preferably *in situ*. The polysilicon is etched back so that its top surface adjoins nitride layer 402. As described above, ~~above~~ a BPSG layer 324 is deposited on the ~~he~~ top surface of the structure and etched back, using an RIE process, or planarized, using a chemical-mechanical polishing technique, until the top surface of BPSG layer 324 is coplanar with the top surface of nitride layer 402, thereby forming a BPSG plug 470. The resulting structure is shown in **Fig. 5B**.

Please replace the paragraph beginning at page 10, line 26, with the following amended paragraph:

As shown in **Fig. 5E**, pad oxide layer 404 is removed, and a P-type dopant is implanted and diffused to adjust the threshold voltage of the MOSFET to be formed. The areas in which this dopant is located are ~~is~~ labeled 417 ~~474~~. An N-type dopant is implanted and diffused to form N+ source layer 476.

Please replace the paragraph beginning at page 13, line 11, with the following amended paragraph:

The use of this process in the basic process sequence shown in **Figs. 5A-5G** produces a similar result, except that, as shown in **Fig. 9, ~~9~~** there is no polysilicon layer 308 on the die surface, only inside the trenches. Therefore, in the three-mask process, N+ polysilicon and BPSG sidewall spacers are formed on the vertical surfaces of BPSG layer

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324 . As mentioned above, a portion of metal layer 326S ~~326~~ (not shown) is used to contact the polysilicon gate 308.

Please replace the paragraph beginning at page 13, line 29, with the following amended paragraph:

If the field shield is contacted in the manner shown in **Fig. 9**, using a wide trench, a termination structure of the kind shown in **Fig. 11** may be employed. In the edge termination region 700, oxide layer 310A, N+ polysilicon layer 308A and three trenches 702A, 702B and 702C are formed by using the trench and contact mask levels. There are no active field plates on the surface of the voltage termination structure shown in **Fig. 11** ~~Fig. 11~~, where the process is reduced to three mask levels. The three trenches 702A, 702B and 702C are typically longitudinal trenches that are parallel to each other and are parallel to and adjacent to an edge of the semiconductor die. Trenches 702A-702C may be formed in the same manner and at the same time as trenches 306 in the active region of the MOSFET (see **Fig. 5B**). The internal structure of trenches 702A-702C is identical to that of trenches 306. Each P-shield region 320 and each polysilicon region 308A "floats" with respect to both source and the drain potentials, because there is no direct electrical contact. Therefore, the three trenches filled with polysilicon 308A, isolated by silicon dioxide layer 310A ~~layer310A~~, act like "floating" p-n junctions (floating rings) with a field plate to reduce the electric field by dividing the voltage among three trenches 702A-702C. Either the P field shield region 320 below each of trenches 702A-702C is in electrical contact with the polysilicon 308A, ~~poly silicon 308A~~ or it is left floating.The contact mask is designed such that a portion 324B of BPSG layer 324 is left over trenches 702A-702C. BPSG layer 324B is removed from the active region of the device side to allow metal layer 326S, which is in contact with the N+ source regions 476, to make contact with P+ region 482. BPSG layer 324B ~~324~~ is also removed from the saw street area of the chip (right side of **Fig. 11**). Polysilicon spacers 478 and BPSG spacers 480 are also shown on the sidewalls of BPSG layer 324B in **Fig. 11**.

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Please replace the paragraph beginning at page 14, line 21, with the following amended paragraph:

Figs. 12A and **12B** illustrate a structure for contacting the gate 308 when the process shown in **Figs. 4A-4H** is used to manufacture the MOSFET. As shown in **Fig. 12A**, oxide layer 404 and ~~are~~ nitride layer 402 are masked so that they are not removed at the point described above (see **Fig. 4B**). Similarly, when the polysilicon layer which will form gate 308 is deposited, and before it is etched back into the trench, the polysilicon layer is masked in the area where the gate contact is to be made, forming polysilicon layer 308B, which is essentially an extension of gate 308 outside the trench. Polysilicon layer 308B is thus in electrical contact with gate 308. BPSG ~~Nitride~~ layer 324 D is an extension of BPSG ~~nitride~~ layer 324. An opening is formed in the contact mask (see **Fig. 4G**) so that when BPSG layer 324D is etched, an opening 710 is formed. When metal layer 326 is deposited, it fills the opening 710 and makes contact with polysilicon layer 308B. The metal mask is configured such that the section of metal layer 326 that contacts polysilicon layer 308B becomes the gate metal portion 326G.

Please replace the paragraph beginning at page 15, line 3, with the following amended paragraph:

Figs. 13A and **13B** illustrate a way of contacting the gate if the process described in **Figs. 5A-5G** is used to manufacture the MOSFET. This process is similar to the one described in **Figs. 5F-5G,** except that polysilicon is inside a wider trench region 306 ~~region, 306W~~.

Please replace the paragraph beginning at page 15, line 6, with the following amended paragraph:

Figs. 14A-14C ~~Figs. 14A-14C~~ illustrate three patterns in which the gate trenches and mesas may be formed: stripe, square and hexagonal geometries. Devices of the present invention may be formed in any of these or other trench layout ~~lay-out~~ patterns.

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Please replace the paragraph beginning at page 15, line 9, with the following amended paragraph:

While specific embodiments of this invention have been described, it should be understood that these embodiment are illustrative, and not limiting. Many other

embodiments according to this invention will be apparent to persons of skill in the art. For example, while the embodiments described above involved MOSFETs, this invention is also applicable to other semiconductor devices, such as trench insulated gate bipolar transistors (IGBTs), vertical power junction field-effect transistors (JFETs) and power bipolar devices. Moreover, while N-channel devices have been described, the ~~these~~ principles of this invention can be used with P-channel devices by reversing the polarities.

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